VMM6210 Datasheet

USB-C Video and Data Hub

PN: 505-001081-01 Rev A

1.1. Introduction

VMM6210 is a highly integrated USB-C alt-mode MST hub featuring HDMI2.1 and DP1.4a audio-video ports. It offers the maximum bandwidth and advanced features from the latest video interface standards. The VMM6210 has a DisplayPort Alt-mode capable USB-C input port, which can receive 2 or 4 lanes of DisplayPort™ video. The analog front end (AFE) with the flexible lane swap option provisions the reversible and flip orientation of standard USB-C connector. The receiver port supports DisplayPort SST/MST input up to HBR3 data rate. DisplayPort MST audio-video streams may be separated to SST and can be converted to HDMI or reconstructed as DP streams and forwarded to the downstream-facing video ports. VMM6210 has one HDMI2.1 transmitter port and a DP++ transmitter port. The HDMI2.1 transmitter supports FRL mode operation up to 12.0 Gbps per lane with 3 or 4 lanes configurations. The DP++ transmitter output is configurable as DP1.4a port or HDMI2.0 port.

VMM6210 transports up to 5 compressed or uncompressed audio-video streams. DSC1.1/1.2a compressed streams can be decoded as DP transport streams or converted into HDMI FRL format. VMM6210 allows DSC pass through of DP steams from the source directly to the connected sinks. The DSC decoder in VMM6210 supports 2:1, 3:1 and the fractional compression ratios of RGB/YCC pixel formats up to 12bpc color depth. It offers secure reception and transmission of high dynamic range content with HDR10, HDR10+ and Dolby Vision™ metadata transport and advanced gaming features. VMM6210 also supports DP1.4a and HDMI2.1 audio stream transports and Dolby ATMOS®, DTS:X® formats.

The VMM6210 includes built-in HW root of trust device security and the industry standard HDCP v1.4/v2.3 AES engine for content protection.

1.2. Features

- Standards compliance/support: USB Type-C, VESA DisplayPort™ v2.0, HDMI2.1, VESA DDM, VESA DSC v1.2a, DP Alt-mode on USB-C v2.0, HDCP v2.3, DisplayID, and EDID v1.6
- Upstream interface
  - USB-C DisplayPort Alt-mode input port
  - Lane swap and flip support
  - DisplayPort™ 1.4a, 4-lane receiver
  - Adaptive receiver equalization (CTLE, DFE)
  - Link clock down-spreading
  - SST/MST transport streams (5 streams)
  - RBR/HBR/HBR2/HBR3 data rate
  - DSC1.1/1.2a or uncompressed video
  - Forward Error Correction (FEC)
  - RGB, YCC444/422/420-pixel formats
  - Video color depth 8, 10, 12 bpc
- Downstream Interfaces
  - 1x HDMI2.1 transmitter port
  - 1x Dual mode transmitter port (DP++)
- HDMI2.1 Transmitter port
  - DC coupled interface
  - FRL mode operation 3 or 4 lanes
  - Max link bandwidth 48 Gbps (3/6/8/10/12G per lane)
  - HDMI 2.0 and 1.4-compliant TMDS operation
  - DSC compressed video pass-through
  - Configurable as single DVI output
  - Static and dynamic HDR10+ metadata
  - Dolby Vision™ metadata in Dolby VSIF
  - Variable Refresh Rate (VRR)
  - Quick Media Switching (QMS)
  - Quick Frame Transport (QFT)
  - Automatic Low Latency Mode (ALLM)
  - Audio 1-32 CH LPCM 192 kHz, HBR up to 1536 kHz, IEC61937 compressed audio
  - Dolby ATMOS, DTS:X formats
  - Consumer Electronics Control (CEC)
- Dual mode (DP++) transmitter port
  - AC coupled interface

  - Static HDR10 and dynamic HDR10+ metadata
  - Dolby Vision metadata in Dolby VSIF
  - Audio 1-32 CH LPCM 192 kHz, HBR up to 1536 kHz, IEC61937 compressed audio
  - DP1.4 mode features:
    - RBR/HBR/HBR2/HBR3 data rate
    - LTTPR mode re-timer
    - Link clock spreading
    - SST or up to 4 MST stream transport
    - DSC compressed video pass-through
    - Forward Error Correction (FEC)
    - Adaptive sync (VRR)
  - HDMI2.0/1.4 TMDS mode features:
    - Max TMDS link bandwidth 18 Gbps
    - Variable Refresh Rate (VRR)
    - Quick Media Switching (QMS)
    - Quick Frame Transport (QFT)
    - Automatic Low Latency Mode (ALLM)
    - Consumer Electronics Control (CEC)
    - Configurable as Single DVI output
- Flexible Connectivity Features
  - CC communication (BMC PD)
  - VBUS detection
  - I²C slave & master interfaces
  - ISP-over-AUX or I2C for firmware update
  - EDID pass-through & I²C mapping via AUX
  - CEC tunneling over AUX channel
  - Dual bank firmware storage for failsafe
  - Internal RGB Test Pattern Generator
- DSC Video Decompression
  - DSC1.1/1.2a decoder (RGB/YCC 444/422/420)
  - Two independent DSC video decoders
  - 1/2/4 DSC slices
  - Max resolution width of 10k
  - 8/10/12 bpc uncompressed data
  - Block prediction support
  - 8 bpc, 8 bpp to 24 bpp with 1/16th resolution
  - 10 bpc, 8 bpp to 30 bpp with 1/16th resolution
  - 12 bpc, 8 bpp to 36 bpp with 1/16th resolution
- Video Pixel Formats & Conversions
  - RGB/YCC color space conversion
  - Programmable coefficient 3x3 matrix
  - YCC 444/422/420 up/down-conversion
- Security Features
  - HDCP v1.4/v2.3repeater
  - Secure firmware download
  - Secure firmware boot
  - Anti-rollback protection
  - Device access protection
  - Debug protection
  - Security asset protection through OTP lock
- Embedded CPU
  - 32-bit RISC-V processor
  - Single/quad SPI Master
  - External 24 MHz XTAL interface
  - I²C master for external device control
  - GPIO interface to MCU
- Power
  - 3.3V IO, 1.8V IO and 0.8V core supplies
  - Low power operation – Deep sleep and Standby states
- ESD
  - 2 kV HBM
  - 250V CDM
  - 100 mA Latch-up
- Package
  - 7 x 7 mm, 100 BGA
  - RoHS compliant
  - Halogen-free IEC 61249-2-21 compliant

1.3. Applications

- USB-C travel dock
- USB-C Digital AV Multiport adapter/dongle
- Digital Signage / Large Format Display
- PC, Notebook Motherboard
- USB-C Alt-mode Mobile PC / Tablet dock
- USB-C / DisplayPort MST hub

Contents

2. Functional Block Diagram

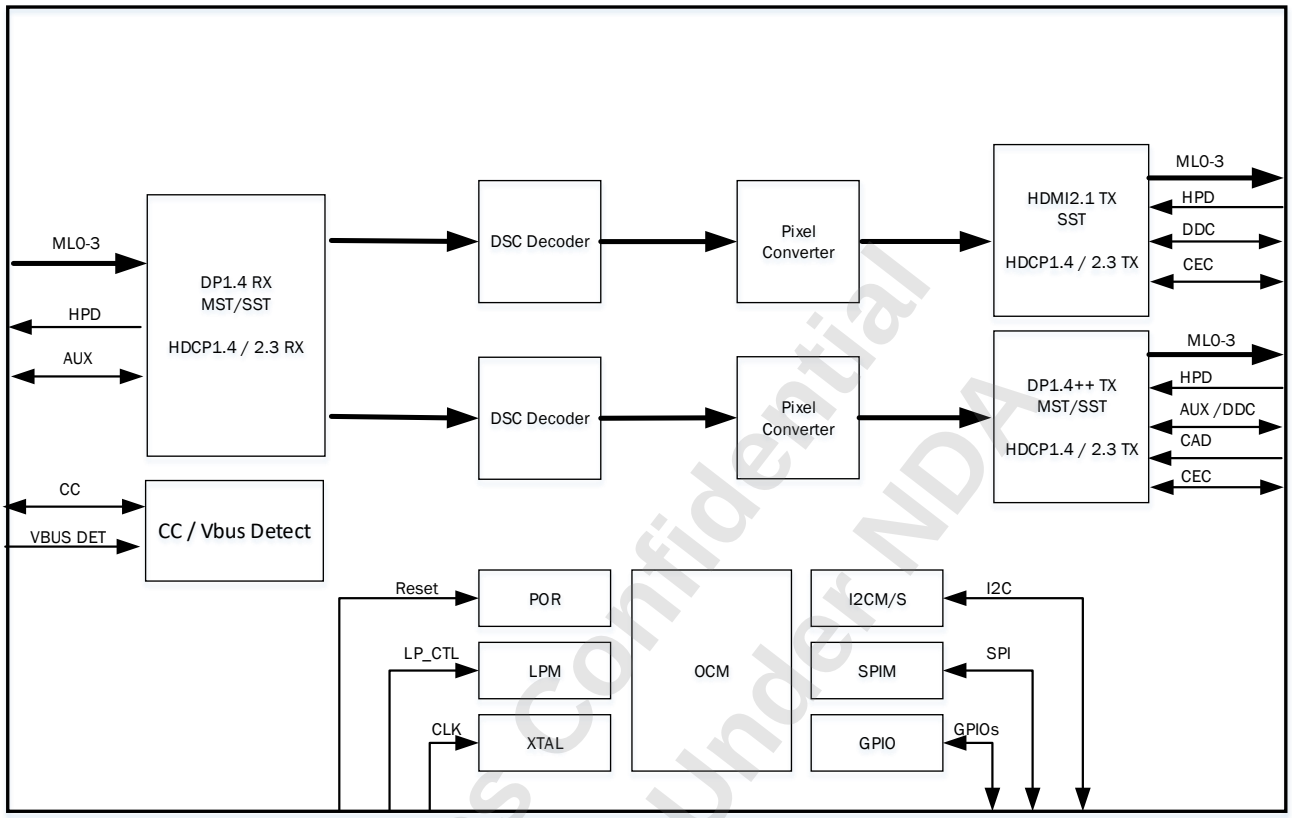

Figure 1. Functional Block Diagram

3. Pin Assignments

3.1. Pinout Drawing – 100 BGA

	1	2	3	4	5	6	7	8	9	10	
A	RxAUXN	RxAUXP	US_TX2P	US_TX2N	US_RX2P	US_RX2N	US_RX1N	US_RX1P	US_TX1N	US_TX1P	A
B	SPIDIO0	RxHPD	RXSRCDET	RSTN_IN	REXT	CC2	CC1	VBUSDET	GPIO10	GPIO07	B
C	XOUT	SPICLK	VDD	VDD18A	VDD18A	VDDA	NC	VDDIO33	GPIO06	GPIO05	C
D	XIN	SPIDIO3	VDD	VDDA	VDDRx	VDDRx	VSS	VDD	GPIO04	GPIO03	D
E	SPIDIO1	SPICSN	VDD	VSS	VSS	VSS	VSS	VDD	GPIO02	GPIO01	E
F	Tx0N0	SPIDIO2	VDDIO33	VSS	VSS	VSS	VSS	VDD	GPIO00	Tx1P0	F
G	Tx0P0	CAD1	VDD18A	VDD18A	VDDTx0	VDDTx1	VDD18A	VDD18A	Tx1HPD	Tx1N0	G
H	Tx0N1	Tx0HPD	VDDA	VDDA	VDDTx0	VDDTx1	VDDA	VDDA	LPCTL	Tx1P1	H
J	Tx0P1	SSDA	SSCL	Tx0DDCSDA	Tx0DDCSCL	Tx1DDCSCL	Tx1DDCSDA	GPIO08	GPIO09	Tx1N1	J
K	Tx0N2	Tx0P2	Tx0N3	Tx0P3	Tx1AUXN	Tx1AUXP	Tx1N3	Tx1P3	Tx1N2	Tx1P2	K
	1	2	3	4	5	6	7	8	9	10	

Figure 2. Pin Assignments 100BGA

3.2. Pin Definitions – 100 BGA

3.2.1. USB Type-C RX Pins I/F

Table 1. USB Type-C RX Pins I/F

Pin Location(s)	Signal	Pin Type	Description
A3	US_TX2P / DP_RX3N	High Speed	Connect to UFP USB-C Differential TX2 P for Type-C connector OR Standard DP Receptacle connector Main Link lane 3 N
A4	US_TX2N / DP_RX3P	High Speed	Connect to UFP USB-C Differential TX2 N for Type-C connector OR Standard DP Receptacle connector Main Link lane 3 P
A5	US_RX2P / DP_RX2N	High Speed	Connect to UFP USB-C Differential RX2 P for Type-C connector OR Standard DP Receptacle connector Main Link lane 2 N

Pin Location(s)	Signal	Pin Type	Description
A6	US_RX2N / DP_RX2P	High Speed	Connect to UFP USB-C Differential RX2 N for Type-C connector OR Standard DP Receptacle connector Main Link lane 2 P
A7	US_RX1N / DP_RX1N	High Speed	Connect to UFP USB-C Differential RX1 N for Type-C connector OR Standard DP Receptacle connector Main Link lane 1 N
A8	US_RX1P / DP_RX1P	High Speed	Connect to UFP USB-C Differential RX1 P for Type-C connector OR Standard DP Receptacle connector Main Link lane 1 P
A9	US_TX1N / DP_RX0N	High Speed	Connect to UFP USB-C Differential TX1 N for Type-C connector OR Standard DP Receptacle connector Main Link lane 0 N
A10	US_TX1P / DP_RX0P	High Speed	Connect to UFP USB-C Differential TX1 P for Type-C connector OR Standard DP Receptacle connector Main Link lane 0 P
A2	RxAUXP	Bidirectional	Connect to DisplayPort RX AUX CH P. Interfacing with UFP USB-C SBU 2 requires external switch or FET
A1	RxAUXN	Bidirectional	Connect to DisplayPort RX AUX CH N. Interfacing with UFP USB-C SBU 1 requires external switch or FET
B3	RxSRCDET	Input	UFP DisplayPort Source Detection
B2	RxHPD	Output	UFP DisplayPort RX Hot-Plug-Detection
B8	VBUSDET	Input	UFP USB-C Vbus Voltage Detector (1.8V tolerant). Use 1:5 ratio external resistor divider for a max Vbus voltage of 5.5V. Connect to GND when not used.
B7	CC1	Bidirectional	UFP USB-C Configuration Channel 1 (3.3V tolerant). Leave NC when not used.
B6	CC2	Bidirectional	UFP USB-C Configuration Channel 2 (3.3V tolerant). Leave NC when not used.

3.2.2. HDMI Tx I/F

Table 2. HDMI Tx I/F

Pin Location(s)	Signal	Pin Type	Description
F1	TX0N0	Output	HDMI Main Link Lane0 N / TMDS CK N
G1	TX0P0	Output	HDMI Main Link Lane0 P / TMDS CK P
H1	TX0N1	Output	HDMI Main Link Lane1 N / TMDS D0 N
J1	TX0P1	Output	HDMI Main Link Lane1 P / TMDS D0 P
K1	TX0N2	Output	HDMI Main Link Lane2 N / TMDS D1 N
K2	TX0P2	Output	HDMI Main Link Lane2 P / TMDS D1 P
K3	TX0N3	Output	HDMI Main Link Lane3 N / TMDS D2 N
K4	TX0P3	Output	HDMI Main Link Lane3 P / TMDS D2 P
H2	TX0HPD	Input	TX0 Hot-Plug-Detect (3.3V tolerant)
J5	Tx0DDCSCL	Output	TX0 DDC clock (open drain, 3.3V tolerant)
J4	Tx0DDCSDA	Bidirectional	TX0 DDC data (open drain, 3.3V tolerant)

3.2.3. DP++ TX I/F

Table 3. DP++ TX I/F

Pin Location(s)	Signal	Pin Type	Description
F10	Tx1P0	Output	TX1 Main Link Lane0 P
G10	Tx1N0	Output	TX1 Main Link Lane0 N
H10	Tx1P1	Output	TX1 Main Link Lane1 P
J10	Tx1N1	Output	TX1 Main Link Lane1 N
K10	Tx1P2	Output	TX1 Main Link Lane2 P
K9	Tx1N2	Output	TX1 Main Link Lane2 N
K8	Tx1P3	Output	TX1 Main Link Lane3 P
K7	Tx1N3	Output	TX1 Main Link Lane3 N
G2	CAD1	Input	TX1 Cable-Adaptor-Detect (external resistor needed)
K5	TX1AUXN	Bidirectional	TX1 AUX CH N
K6	TX1AUXP	Bidirectional	TX1 AUX CH P
G9	TX1HPD	Input	TX1 Hot-Plug-Detect (3.3V tolerant)
J6	Tx1DDCSCL	Output	TX1 DDC clock (open drain, 3.3V tolerant)
J7	Tx1DDCSDA	Bidirectional	TX1 DDC data (open drain, 3.3V tolerant)

3.2.4. Control Pins

Table 4. Control Pins

Pin Location(s)	Signal	Pin Type	Description
B4	RSTN_IN	Input	External reset (internal pull-up, Schmitt trigger)
D1	XIN	Input	Reference crystal clock input (24 MHz)
C1	XOUT	Output	Reference crystal clock output
J3	SSCL	Bidirectional	I2C slave clock (open drain), Connect to 3V3 pull-up when not used
J2	SSDA	Bidirectional	I2C slave data (open drain), Connect to 3V3 pull-up when not used
E2	SPICSN	Output	Serial Flash Chip Enable
C2	SPICLK	Output	Serial Flash Clock
B1	SPIDIO0	Bidirectional	Serial Flash Data Input 0
E1	SPIDIO1	Bidirectional	Serial Flash Data Input 1
F2	SPIDIO2	Bidirectional	Serial Flash Data Input 2
D2	SPIDIO3	Bidirectional	Serial Flash Data Input 3
H9	LP_CTL	Input	Low Power Mode Control (active Low, by default)

Pin Location(s)	Signal	Pin Type	Description
B5	REXT	Input	Connect to External Resistor (12K ohm, 1% accuracy)

3.2.5. GPIOs

Table 5. GPIOs

Pin Location(s)	Signal	Pin Type	Description
F9	GPIO00	Bidirectional	General purpose input/output (Internal Pull-down)
E10	GPIO01	Bidirectional	General purpose input/output (Internal Pull-down)
E9	GPIO02	Bidirectional	General purpose input/output (Internal Pull-down)
D10	GPIO03	Bidirectional	General purpose input/output (Internal Pull-down)
D9	GPIO04	Bidirectional	General purpose input/output (Internal Pull-down)
C10	GPIO05	Bidirectional	General purpose input/output (Internal Pull-down)
C9	GPIO06	Bidirectional	General purpose input/output (Internal Pull-down)
B10	GPIO07	Bidirectional	General purpose input/output (Internal Pull-down)
J8	GPIO08	Bidirectional	General purpose input/output (Open-drain, recommended for CEC)
J9	GPIO09	Bidirectional	General purpose input/output (Open-drain, recommended for CEC)
B9	GPIO10	Bidirectional	General purpose input/output (Internal Pull-down)

Note: GPIOs can be NC when not used.

3.2.6. Power

Table 6. Power

Pin Location(s)	Signal	Pin Type	Description
C3,D3,D8,E3,E8,F8	VDD	Power	0.8V digital core supply
D5,D6	VDDRx	Power	0.8V Receiver power supply
G5,H5	VDDTx0	Power	0.8V HDMI Transmitter power supply
G6,H6	VDDTx1	Power	0.8V DP Transmitter power supply
C6,D4,H3,H4,H7,H8	VDDA	Power	0.8V Analog power supply
C4,C5,G3,G4,G7,G8	VDD18A	Power	1.8V Analog power supply
C8,F3	VDDIO33	Power	3.3V IO power supply

3.2.7. Ground

Table 7. Ground

Pin Location(s)	Signal	Pin Type	Description
D7,E4,E5,E6,E7,F4,F5,F6,F7	VSS	Power	Ground

3.2.8. NC

Table 8. NC

Pin Location(s)	Signal	Pin Type	Description
C7	NC	—	Do not connect

Note:

- If using TX1 port as DP++, add 1 MΩ pull-down resistor on CAD1
- If using TX1 port as HDMI, add 100 kΩ pull-up resistor on CAD1

4. Application Configurations

4.1. Bootstrap Configurations

Table 9. VMM6210 bootstrap configurations

GPIO #	Function Mode	Function Description	Default Value
1:0	Boot mode	00 : Normal (300 MHz MCU, 50 MHz SPI) 01 : Failsafe (24 MHz MCU, 6 MHz SPI) 10 : SPI bypass mode 11 : Service mode	00
2	Internal USB CC mode	0 : CC Disabled 1 : CC Enabled	0
3	Firmware Offset	0 : Flash Offset 0x0~0xFFFFF 1 : Flash Offset 0x100000~0x1FFFFF	0

Note: Minimum storage size requirement is 1024K Bytes (8M bits).

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Table 10. VMM6210 absolute maximum ratings

Parameter	Min	Max	Units
0.8V supply voltage	-0.3	0.88	V
1.8V supply voltage	-0.3	1.98	V
3.3V supply voltage	-0.3	3.63	V
Storage temperature, unbiased	-55	150	°C
Operating temperature (Ta)	0	70	°C
Junction temperature (Tj)	—	125	°C
Lead soldering temperature (10 seconds)	—	260	°C
Input current at any pin (EIA/ JESD78 latch-up)	—	100	mA
ESD rating, HBM	—	±2	kV
ESD rating, CDM	—	±250	V

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.2. DC Specification

Table 11. VMM6210 DC Specification

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage	-	—	0.96	V
V_{IH}	Input high voltage	2.45	—	—	V
V_{hys}	Hysteresis	100	—	—	mV
I_{PU}	Input weak pullup current (PAD @ 0V)	20	—	100	uA
I_{PD}	Input weak pulldown current (PAD @ VDDIO)	20	—	100	uA
R_{PU}	Internal pull-up resistor value	36.9	—	88.54	kΩ
R_{PD}	Internal pull-down resistor value	20.53	—	70.98	kΩ
V_{OL}	Output low voltage (@ 12mA IOL)	—	—	0.6	V
V_{OH}	Output high voltage (@ 12mA IOH)	2.4	—	—	V

Note: These IOs have configurable max drive strength of 2 mA, 4 mA, 8 mA, 12 mA.

Table 12. DC Specification I2C IOs (Open-Drain)

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage	-0.3	–	0.89	V
V_{IH}	Input high voltage	2.55	–	–	V
V_{hys}	Hysteresis	297	–	–	mV
V_{OL}	Output low voltage	–	–	0.4	V
V_{OH}	Output high voltage	2.7	–	–	V

Table 13. DC Specification XTAL IOs (1.8V)

Symbol	Parameter	Min	Typ	Max	Units
V_{IL}	Input low voltage	-0.1	–	0.49	V
V_{IH}	Input high voltage	1.4	–	–	V

5.2.1. DisplayPort Interface DC Specification

The VESA DisplayPort related DC specification is compliant with the VESA DisplayPort Standard v1.1a/v1.2/v1.4.

5.2.2. Power Supply DC Specification

Table 14. Power Supply DC Specification

Parameter	Min	Typ	Max	Units
0.8V power supply	0.76	0.8	0.84	V
1.8B power supply	1.62	1.8	1.98	V
3.3V power supply	2.97	3.3	3.63	V

5.3. AC Specification

5.3.1. DisplayPort Interface AC Specification

The VESA DisplayPort related AC specification is compliant with the VESA DisplayPort Standard v1.1a/v1.2/v1.4.

5.3.2. I²C SCL/SDA Specification

DDC and I²C AC/DC specification is compliant with the standard I²C specification.

5.3.3. SPI Specification

SPI interface AC/DC specification is compliant with Standard SPI specification. Maximum SPI clock frequency supported is 50 MHz.

5.3.4. Crystal Oscillator Interface AC Specification

Table 15. Crystal Oscillator Interface AC Specification

Symbol	Parameter	Min	Typ	Max	Units
F_c	Clock Frequency	—	24	—	MHz
T_{cc}	Clock frequency tolerance	-100	—	+100	ppm

5.4. Power Consumption

Table 16. Active Mode power consumption

Parameter	Typ	Max	Units
MST to 2x SST conversion w/o DSC: Input Config: DP 4 L HBR3, Output1 config: HDMI2.1 FRL 4L 12G, Output2 config DP 4L HBR3			
0.8V supply	865	1150	mA
1.8V supply	35	50	mA
3.3V supply	4	6	mA
MST to 2x SST conversion w/ DSC: Input Config: DP 4 L HBR3, Output1 config: HDMI2.1 FRL 4L 12G, Output2 config DP 4L HBR3			
0.8V supply	880	1250	mA
1.8V supply	35	50	mA
3.3V supply	4	6	mA
MST to 2x SST conversion w/ DSC: Input Config: DP 2 L HBR3, Output1 config: HDMI2.1 FRL 4L 12G, Output2 config DP 4L HBR3			
0.8V supply	760	1120	mA
1.8V supply	35	50	mA
3.3V supply	4	6	mA

Note:

- Typ condition is 0.8V/1.8V/3.3V supply, room temperature.
- Max condition is 0.84V/1.98V/3.63V supply, 70°C ambient

Table 17. Low Power Mode Power Consumption

Parameter	Typ	Max	Units
Deep Sleep: Device wakes up upon HPD detection			
0.8V supply	7.5	—	mA
1.8V operation	2	—	mA
3.3V operation	2	—	mA

Note:

- Typ condition is 0.8V/1.8V/3.3V supply, room temperature.
- Max condition is 0.84V/1.98V/3.63V supply, 70°C ambient Thermal Specification

Table 18. Thermal Specification

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Junction temperature	T_J	Still air	—	—	125	°C
Thermal resistance – junction to ambient -143 BGA package	Θ_{JA}	Still air	—	28.9	—	°C/W
Thermal resistance – junction to case -143 BGA package	Θ_{JC}	Still air	—	13.09	—	°C/W
Thermal resistance – junction to board -143 BGA package	Θ_{JB}	Still air	—	14.92	—	°C/W
Thermal resistance – junction to ambient -100 BGA package	Θ_{JA}	Still air	—	32.3	—	°C/W
Thermal resistance – junction to case -100 BGA package	Θ_{JC}	Still air	—	14.66	—	°C/W
Thermal resistance – junction to board -100 BGA package	Θ_{JB}	Still air	—	17.04	—	°C/W

6. Layout Guidelines

6.1. Layer Stack-up

- Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the hub inputs and from the hub output to the subsequent receiver circuit.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission-line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the fast-edged control signals on the bottom layer prevents cross-talk into the high-speed signal traces and minimizes EMI.

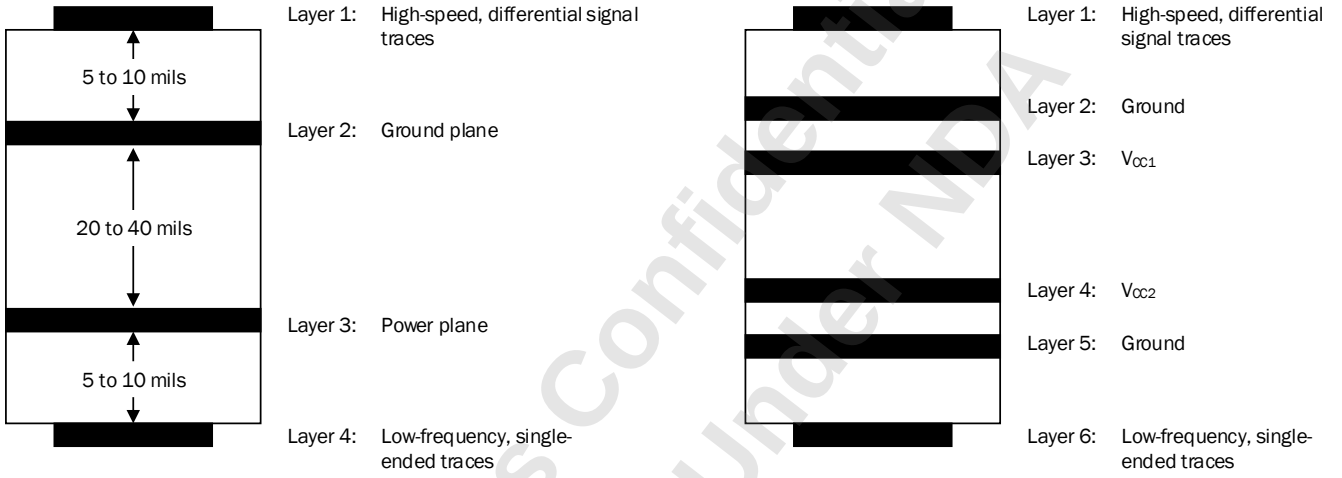

Figure 3. Recommended 4- or 6-Layer (0.062") Stack-up for a Receiver PCB Design

6.2. Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and minimize EMI.

- Select proper PCB stack up and trace width at 100Ω differential transmission line impedance for the high-speed DP/TMDS/FRL signals
  - RXP/N and TXP/N pairs should be routed with controlled 100Ω differential impedance (±15%).
  - For 100Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
  - Route all differential pairs on the same layer.
  - Keep away from other high-speed signals.
- Minimize intra-pair and inter-pair trace lengths within each differential pair.
  - Intra-pair routing should be kept to within 2 mils.
  - Reduce inter-pair skew, caused by component placement and IC pinouts.
  - Each pair should be separated at least by 3 times the signal trace width.
- Use 45° bends (chamfered corners), instead of right-angle (90°) bends.
  - Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities.
  - A 45° bend is seen as a smaller discontinuity.
- When routing around an object, route both traces of a pair in parallel.
  - Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
- Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other.

- 0402 size is recommended; 0603 size is acceptable; 0805 size is not allowed.
- When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane underneath.
- Avoid metal layers and traces underneath or between the pads of the DisplayPort connectors for better
- impedance matching, otherwise they will cause the differential impedance to drop below 75Ω and cause the board to fail during TDR testing.
- Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100Ω differential impedance.
  - Large vias and pads can cause the impedance to drop outside the required range (100Ω ± 15%).
  - The number of vias should be kept to a minimum. It is recommended to keep the via count to two or fewer.
- Use solid power and ground planes for 100Ω impedance control and minimum power noise.
  - Keep traces on layers adjacent to ground plane.
  - Do NOT route differential pairs over any plane split.
- Keep the trace length between the DisplayPort connector and the hub device as short as possible to minimize attenuation.
  - Keep the RX trace length < 4" with IL < 4 dB @4.05 GHz from DP connector to hub.
  - Keep the TX trace length < 6" with IL < 6 dB @4.05 GHz from hub to DP connector.
- Use good DisplayPort connectors whose impedances meet the specifications.
- Adding test points will cause impedance discontinuity, and therefore negatively impact signal performance.
  - If test points are used, they should be placed in series and symmetrically.
  - They must not be placed in a manner that causes a stub on the differential pair.

6.3. Filtering Capacitors

- Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
- Place smaller 0.1 µF or 0.01 µF capacitors close to the hub device.

7. Package and Ordering Information

7.1. Package Outline Drawing – 100 BGA

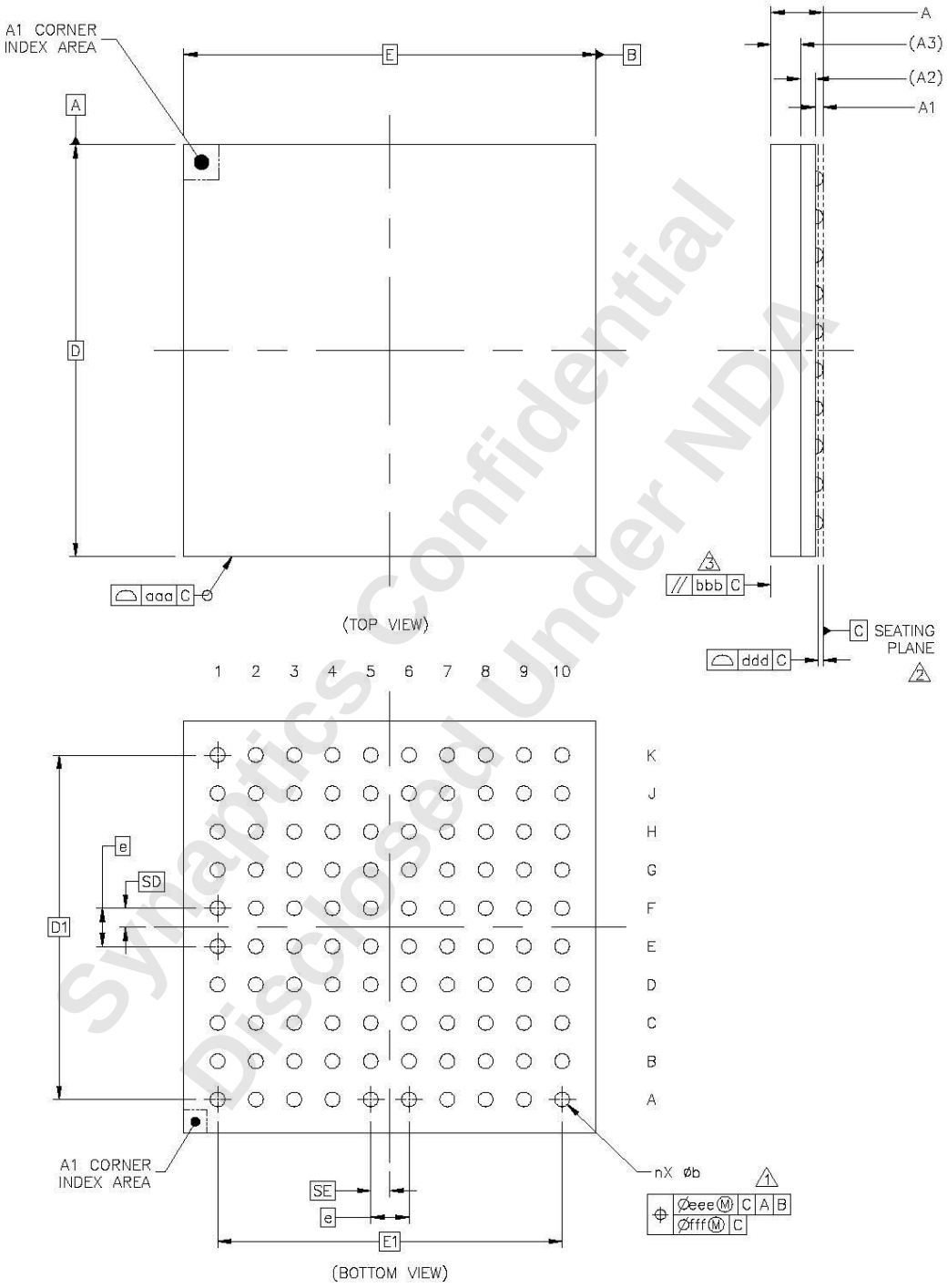

Figure 4. 100 BGA

- Dimension b is measured at the maximum solder ball diameter, parallel to datum plane C.
- Datum C (seating plane) is defined by the spherical crowns of the solder balls.
- Parallelism measurement shall exclude any effect of mark on top surface of package.

7.2. Dimensions - 100 BGA

All measurements are in millimeters unless otherwise specified.

Table 19. Package dimensions

Dimension	Symbol	Minimum	Typical	Maximum
Total thickness	A	0.85	0.885	0.96
Stand off	A1	0.085	0.135	0.185
Substrate thickness	A2		0.25 REF	
Mold thickness	A3		0.50 REF	
Body size	D		7.00 BSC	
	E		7.00 BSC	
Ball width	b	0.225	0.25	0.275
Ball diameter			0.23	
Ball opening			0.25	
Ball pitch	e		0.65 BSC	
Ball count	n		100	
Edge ball center to center	D1		5.85 BSC	
	E1		5.85 BSC	
Body center to contact ball	SD		0.325 BSC	
	SE		0.325 BSC	
Package edge tolerance	aaa		0.1	
Mold flatness	bbb		0.1	
Coplanarity	ddd		0.08	
Ball offset (package)	eee		0.15	
Ball offset (ball)	Fff		0.08	

7.3. Package Marking

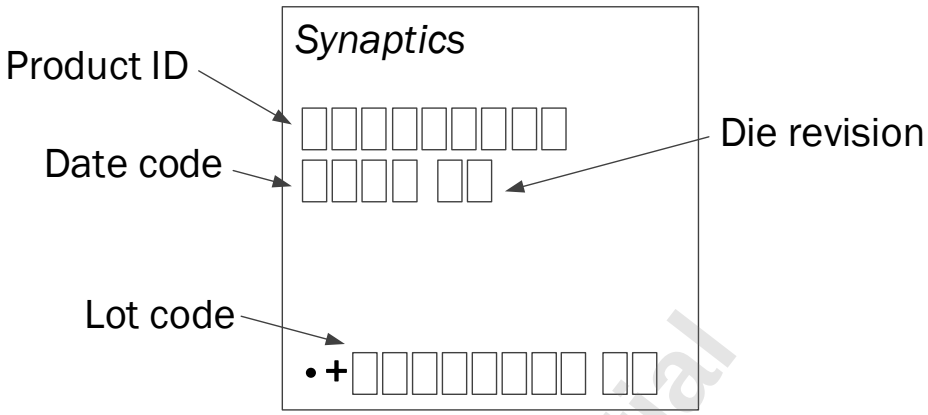

Figure 5. Package Marking

7.4. Ordering information

Table 20. Part numbers for ordering

Ordering code	Package description	Shipping
VMM6210BYF-T (Rev A0)	100-contact BGA, 7 x 7 mm	Trays
VMM6210BYF-R (Rev A0)	100-contact BGA, 7 x 7 mm	Tape and reel
VMM6210BYFB0-T (Rev B0)	100-contact BGA, 7 x 7 mm	Trays
VMM6210BYFB0-R (Rev B0)	100-contact BGA, 7 x 7 mm	Tape and reel
VMM6210BYFB1-T (Rev B1)	100-contact BGA, 7 x 7 mm	Trays
VMM6210BYFB1-R (Rev B1)	100-contact BGA, 7 x 7 mm	Tape and reel

Note: Tape and reel only available for volume shipments.

7.5. Environmental and Regulatory Compliance

This Synaptics product is built in compliance with the RoHS directive and the *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01). This Synaptics product is also Halogen-Free (HF) compliant.

8. Reference Documents

- *Synaptics Quality Specification: Environmental Conservation Program* (PN: 526-000223-01)

9. Revision History

Revision	Description
1	Initial release
2	Updated Functional Block diagram, Power supply grouping, DC characteristics. Minor updates to Introduction and Features.
3	Updated some pin descriptions. Updated Package drawing. Updated absolute maximum ratings in Table 10.
4	Updated with second package information (7x7mm 100BGA) and ordering information
5	Added power consumption data, thermal specification and ordering information for rev B0. Updated the package outline dimensions.
6	Deprecated 143BGA package. Minor update in Table 1 and updated ordering information (Table 20).
A	RTP

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